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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,078	08/30/2001	Todd R. Abbott	MIO 0083 PA	7688

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EXAMINER
KIELIN, ERIK J

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,078	ABBOTT, TODD R.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the c ver she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-16,39 and 45-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,10,15 and 45-49* is/are rejected.

7)☒ Claim(s) *7,9,11,14,16 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action responds to the Amendment filed 25 April 2003.

Drawings

1. The corrected or substitute drawings were received on 25 April 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 8, 10, 15, and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,548,871 B1 (**Horita** et al.) in view of US 6,037,248 (**Ahn**).

Regarding claim 1, **Horita** discloses a method of fabricating a semiconductor device comprising:

forming a first dielectric layer **8a, 8b, 44, 46** over a base substrate **1** (Fig. 16);

forming a damascene trench **22, 23, 24** in said first dielectric layer **8a, 8b, 44, 46** said trench having a gate area and a local interconnect area (Fig. 17, col. 17, lines 33-60 and Fig. 20; col. 1, lines 50-60);

forming a gate oxide layer **3** on said base substrate **1** within said gate area of said damascene trench **23** (Figs. 18);

depositing a conductive layer **42** over said base substrate **1** such that said damascene trench **22, 23, 24** is filled with a conductive material **42** (Fig. 18; col. 18, lines 14-21);

planarizing said device to define a damascene structure including a damascene gate structure **61** and a damascene local interconnect structure **65** electrically coupled by said conductive material within said damascene trench **71, 72,** wherein said damascene local interconnect structure forms a connection to said base substrate (Figs. 11, 19, 20; col. 18, lines 22-27).

(See also col. 14, line 6- to col. 18, line 64.)

Horita does not teach removing the first dielectric layer **8a, 8b, 44, 46**.

Ahn teaches the benefits of removing the first dielectric layer to have an air dielectric **56** around the gate structure **33, 36, 37** and the interconnect structure **48, 53, 54, 72, etcetera** to reduce the capacitance and the RC delay associated therewith (Abstract; col. 5, lines 43-46).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to remove the dielectric layer of **Horita**, as taught by **Ahn** to reduce RC delay.

Regarding claim 2, **Horita** discloses the isolation trench **2** formed before the dielectric layer **8a, 8b, 44, 46** (Fig. 12).

Regarding claim 3, **Horita** discloses the trenches **22, 23, 24** partially overlie the isolation trench **2** (Figs. 18, 19, and 20).

Regarding claim 4, **Horita** discloses that the element isolation is a "trench type element" indicating that a trench is formed by etching into the base substrate **1** and filling with the dielectric material **2** (col. 12, lines 32-40).

Regarding claim 5, the **Horita** Figs. show that the dielectric layer **8a, 8b, 44, 46** is conformal because it conforms to the surface of the base substrate **1**.

Regarding claim 6, **Horita** discloses that photolithography and dry etching are used to form the openings 22, 23, 24 (col. 17, lines 33-35). Accordingly, it is seen to be inherent that a patterned mask is formed over the dielectric layer 46 (i.e. photolithography) and that the mask is stripped afterward because no mask is shown to be left on the finally patterned dielectric layer 46.

Regarding claim 8, **Horita** discloses that the gate oxide layer 32 formation comprises,

growing an oxide layer 32 (Fig. 12) on said base substrate 1;

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer within said local interconnect region (compare to Figs. 18 and 20 wherein the local interconnect region is shown);

etching away the exposed portion of said oxide layer and stripping the mask (col. 16, first paragraph).

Regarding claim 10, **Horita** discloses the conductive material comprises polysilicon (col. 15, lines 61-62).

Regarding claim 15, **Horita** discloses spacers 6 formed against the vertical walls of said damascene gate and local interconnect structures Fig. 11.

Regarding claim 45, **Horita** discloses the local interconnect **14, 15**, area partially overlies an isolation trench **2** (Fig. 11; also shown in Figs. 19, 20).

Regarding claims 46 and 47, **Horita** discloses that there are plural gate areas and plural local interconnect areas in the trenches (Figs. 11, 19, and 20).

Regarding claim 48, **Horita** discloses the isolation trench **2** is shown to be a shallow isolation trench.

Regarding claim 49, **Horita** discloses the gate area and the local interconnect area of the damascene trench are formed by said patterned mask and etching (Figs. 11, 19, and 20).

Allowable Subject Matter

4. Claim 39 is allowed.

5. Claims 7, 9, 11, 14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 7, 9 and 39, the prior art does not teach or suggest, in combination with the other claimed limitations, that there is an implant formed within the opening of the damascene trench into the base substrate.

Regarding claim 11, the prior art does not teach or suggest, in combination with the other claimed limitations, that a silicide layer is formed over the polysilicon material within the trench. Moreover **Horita** teaches away from this at col. 1, lines 25-39.

Regarding claims 14 and 16, the applied art does not teach or suggest in proper combination with the other claimed features, that the lightly-doped drain regions are formed *after* the removal of the dielectric layer. Such would be at best obvious to try in the applied references.

Response to Arguments

7. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
July 3, 2003